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**Lab 4 Report**

**Hierarchical Design of a CLA Adder**

**Date \_\_\_\_3/11/17\_\_\_\_\_\_\_\_\_**

**by**

**Name \_\_\_Anahit Sarao\_\_\_ SID \_\_\_008435583\_\_\_\_\_**

**Name \_\_\_\_Maxwell Chesier\_\_\_\_\_ SID \_\_\_\_009193717\_\_\_**

**Lab Record**

|  |  |  |  |
| --- | --- | --- | --- |
| **Tasks** | **Designed by (print name)** | **Verified by (print name)** | **\*Completion Status** |
| **1** | Anahit | Ryan | B |
| **2** | Maxwell | Ryan | X |

|  |  |  |  |
| --- | --- | --- | --- |
| **Task** | **Performed by (print name)** | **Validated by (print name)** | **\*Completion Status** |
| **3** | **N/A** | Ryan | **X** |

**San Jose State University**

**Department of Computer Engineering**

**CMPE 125 Spring 2017**